

NEW JEDEC SDRAM MODULE

KMM366S1623AT

KMM366S1623AT SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S1623AT is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S1623AT consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM366S1623AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S1623AT-G8	125MHz (8ns)
KMM366S1623AT-G0	100MHz (10ns)
KMM366S1623AT-G2	83MHz (12ns)
- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V**0.3V power supply
- WCBR cycle with address key programs
 - Latency (Access from column address)
 - Burst Length (1, 2, 4, 8 & Full page)
 - Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : Height(1,250mil), double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50		
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51		
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD		
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52		
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC		
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF		
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC		
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss		
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53		
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54		
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55		
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss		
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56		
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57		
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58		
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59		
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD		
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60		
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61		
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62		
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63		
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss		
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3		
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC		
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0		
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1		
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2		
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD		

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
CS0 ~ CS3	Chip Select Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No Connection

- * These pins are not used in this module.
- ** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System Clock	Active on the positive going edge to sample all inputs.
\overline{CS}	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Colck Enable	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
\overline{RAS}	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with \overline{CAS} low. Enables column access.
\overline{WE}	Write Enable	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
DQM0 ~ 7	Data Input/Output Mask	Makes data output Hi-Z, tSHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.

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SERIAL PRESENCE DETECT INFORMATION

- Serial PD interface Protocol : IIC
- Current sink capability of SDA driver **3mA
- Maximum colck frequency : 80KHz
- Contents :

Byte #	Function described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	2
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	2
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	2
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	2
31	Module bank density	2 banks of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	Initial release			00h			
63	Checksum for bytes 0 ~ 62	-			00h			
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			



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SERIAL PRESENCE DETECT INFORMATION (Continued)

Byte #	Function described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78 Manufacturer part # (Data bits)	6			36h			
79 Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82 Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Composition component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			00h			
94	Manufacturing date (Year)	-			00h			
95-98	Assembly serial #	-			00h			
99-125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select addresses are excluded in counting the total # of addresses.
 2. This value is based on the component specification.

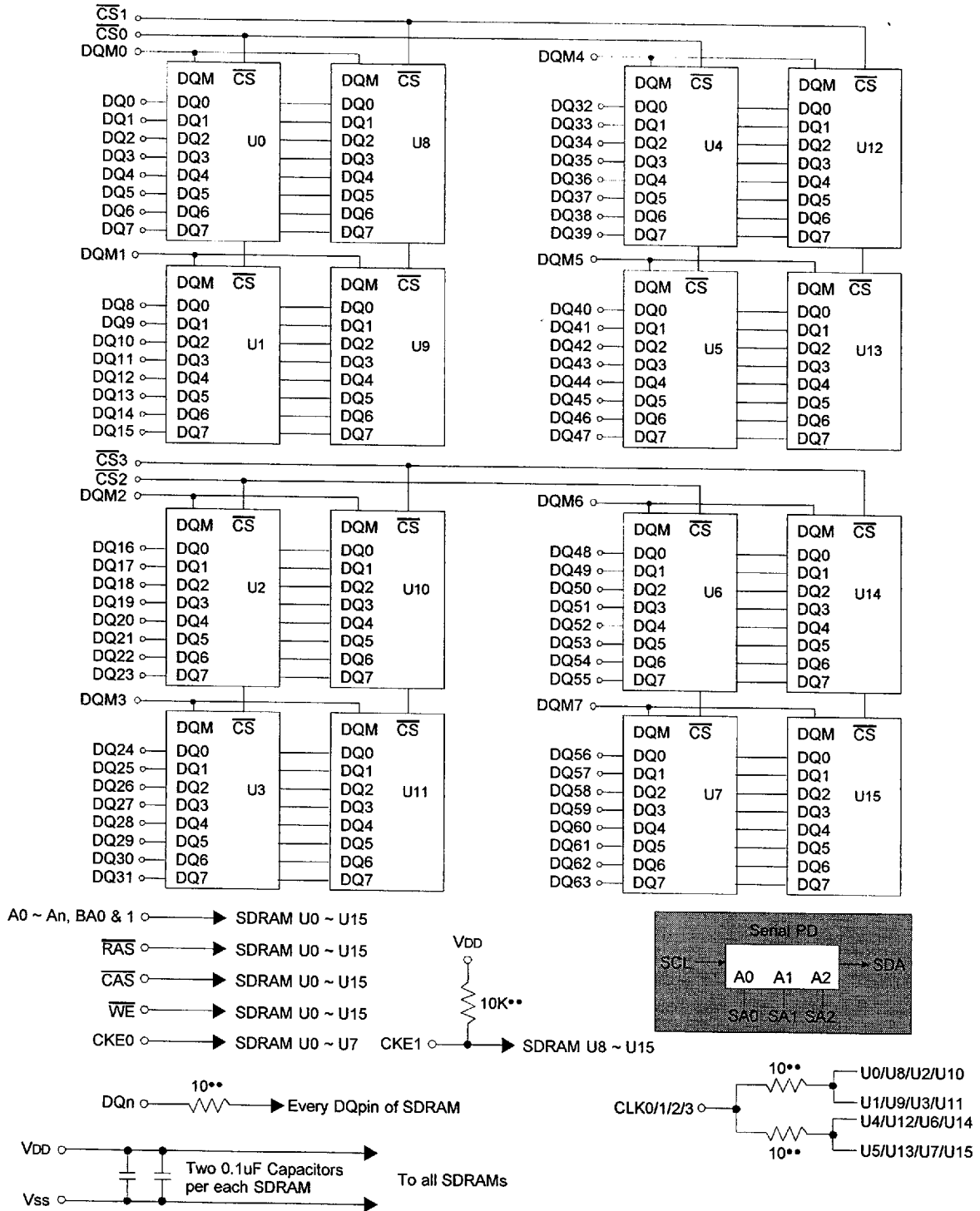


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FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	**
Power dissipation	PD	16	W
Short circuit current	IOS	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70**)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	VIH	2.0	3.0	VDD+0.3	V	1
Input low voltage	VIL	-0.3	0	0.8	V	2
Output high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output low voltage	VOL	-	-	0.4	V	IOL = 2mA
Input leakage current	IIL	-80	-	80	uA	3
Output leakage current	IOL	-10	-	10	uA	4

Note : 1. VIH (max) = 4.6V AC for pulse width **10ns acceptable.
 2. VIL (min) = -1.5V AC for pulse width **10ns acceptable.
 3. Any input 0V ** VIN ** VDD + 0.3V, all other pins are not under test = 0V
 4. Dout is disabled, 0V ** VOUT ** VDD

CAPACITANCE (TA = 25**, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	CIN1	-	90	pF
Input capacitance (RAS, CAS, WE)	CIN2	-	90	pF
Input capacitance (CKE0 ~ CKE1)	CIN3	-	55	pF
Input capacitance (CLK0 ~ CLK3)	CIN4	-	40	pF
Input capacitance (CS0 ~ CS3)	CIN5	-	35	pF
Input capacitance (DQM0 ~ DQM7)	CIN6	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	COU	-	25	pF



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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	ICC1	Burst Length = 1 tRC**trC(min) IOL = 0 mA		1,240	1,020	960	mA	1
Precharge Standby Current in power-down mode	ICC2P	CKE**VIL(max), tCC = 15ns		32			mA	
	ICC2PS	CKE & CLK**VIL(max), tCC = **		32				
Precharge Standby Current in non power-down mode	ICC2N	CKE**VIH(min), \overline{CS} **VIH(min), tCC = 15ns Input signals are changed one time during 30ns		480			mA	
	ICC2NS	CKE**VIH(min), CLK**VIL(max), tCC = ** Input signals are stable		320				
Active Standby Current in power-down mode	ICC3P	CKE**VIL(max), tCC = 15ns		96			mA	
	ICC3PS	CKE & CLK**VIL(max), tCC = **		96				
Active Standby Current in non power-down mode (One Bank Active)	ICC3N	CKE**VIH(min), \overline{CS} **VIH(min), tCC = 15ns Input signals are changed one time during 30ns		640			mA	
	ICC3NS	CKE**VIH(min), CLK**VIL(max), tCC = ** Input signals are stable		400				
Operating Current (Burst Mode)	ICC4	IOL = 0 mA Page Burst 2 Banks activated tCCD = 2CLKs	3	1,600	1,320	1,160	mA	1
			2	1,160	1,080	1,000		
Refresh Current	ICC5	tRC**trC(min)		2,880			mA	2
Self Refresh Current	ICC6	CKE**0.2V		24			mA	

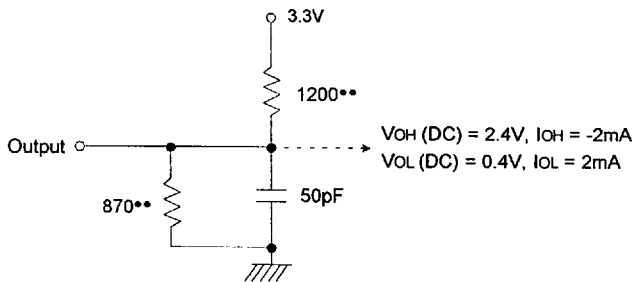
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

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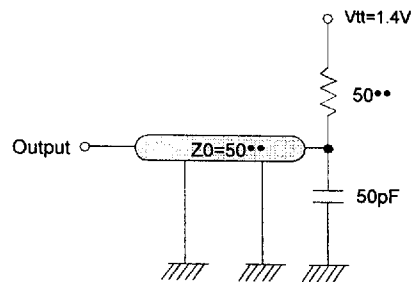
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AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V^{••} ± 0.3V, T_A = 0 to 70^{••})

Parameter	Value	Unit
AC Input levels (V _{IH} /V _{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t _r / t _f = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note	
		-8	-10	-12			
Row active to row active delay	t _{RRD} (min)	16	20	24	ns	1	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t _{RCD} (min)	20	24	26	ns	1	
Row precharge time	t _{RP} (min)	20	24	26	ns	1	
Row active time	t _{RAS} (min)	48	50	60	ns	1	
	t _{RAS} (max)	100			us		
Row cycle time	@Operation	t _{RC} (min)	70	80	90	ns	1
	@Auto refresh	t _{RC1} (min)	80	80	90	ns	1
Last data in to new col. address delay	t _{CDL} (min)	1			CLK	2	
Last data in to row precharge	t _{RDL} (min)	1			CLK	2	
Last data in to burst stop	t _{BDL} (min)	1			CLK	2	
Col. address to col. address delay	t _{CCD} (min)	1			CLK	3	
Number of valid output data	CAS latency=3		2		ea	4	
	CAS latency=2		1				

- Note :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

- Note :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf)=1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.



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FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S1623AT- G8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S1623AT- G0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S1623AT- G2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1



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SIMPLIFIED TRUTH TABLE

COMMAND		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2	
Refresh	Auto Refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self Refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.		H	X	L	L	H	H	X	V	Row Address			
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4	
	Auto Precharge Enable									H		4, 5	
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4	
	Auto Precharge Enable									H		4, 5	
Burst Stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L	X		
	All Banks								X	H			
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X				
	Exit			L	H	X	X					X	X
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	L	H	H	X	X	X	X					
				L	V	V	V						
DQM		H	X					V	X		7		
No Operation Command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at trp after the end of burst.

6. Burst stop command is valid at every burst length.

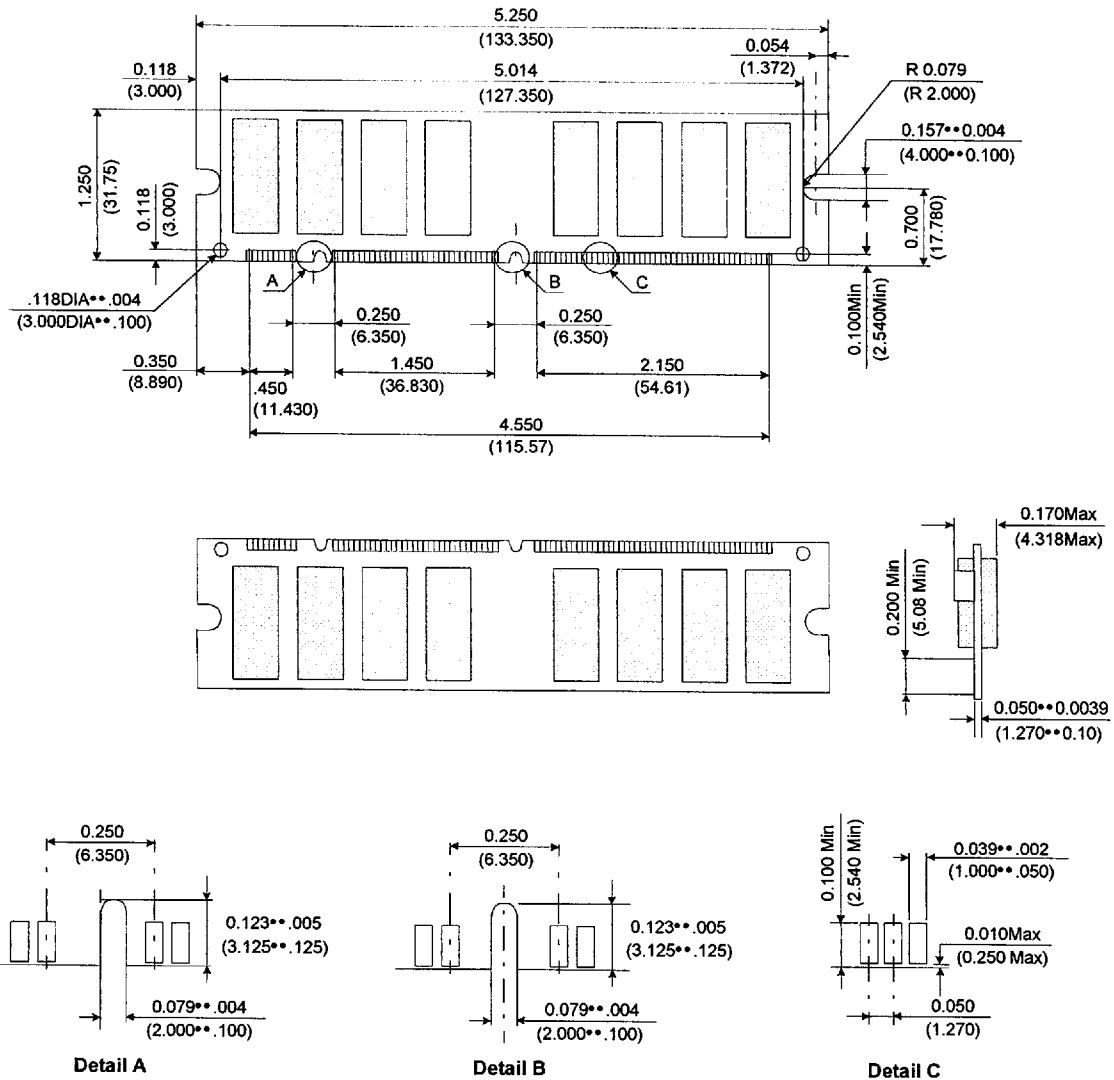
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

NEW JEDEC SDRAM MODULE

KMM366S1623AT

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT



REV. 1 Jan. '97